7SG1641 Ohmega 402 50

Distance Protection Relay

Document Release History

This document is issue 2010/02. The list of revisions up to and including this issue is:
Pre release

2010/02	Document reformat due to rebrand

Software Revision History

2004/03	2615H80031R21	

Contents

1 Relay Connections

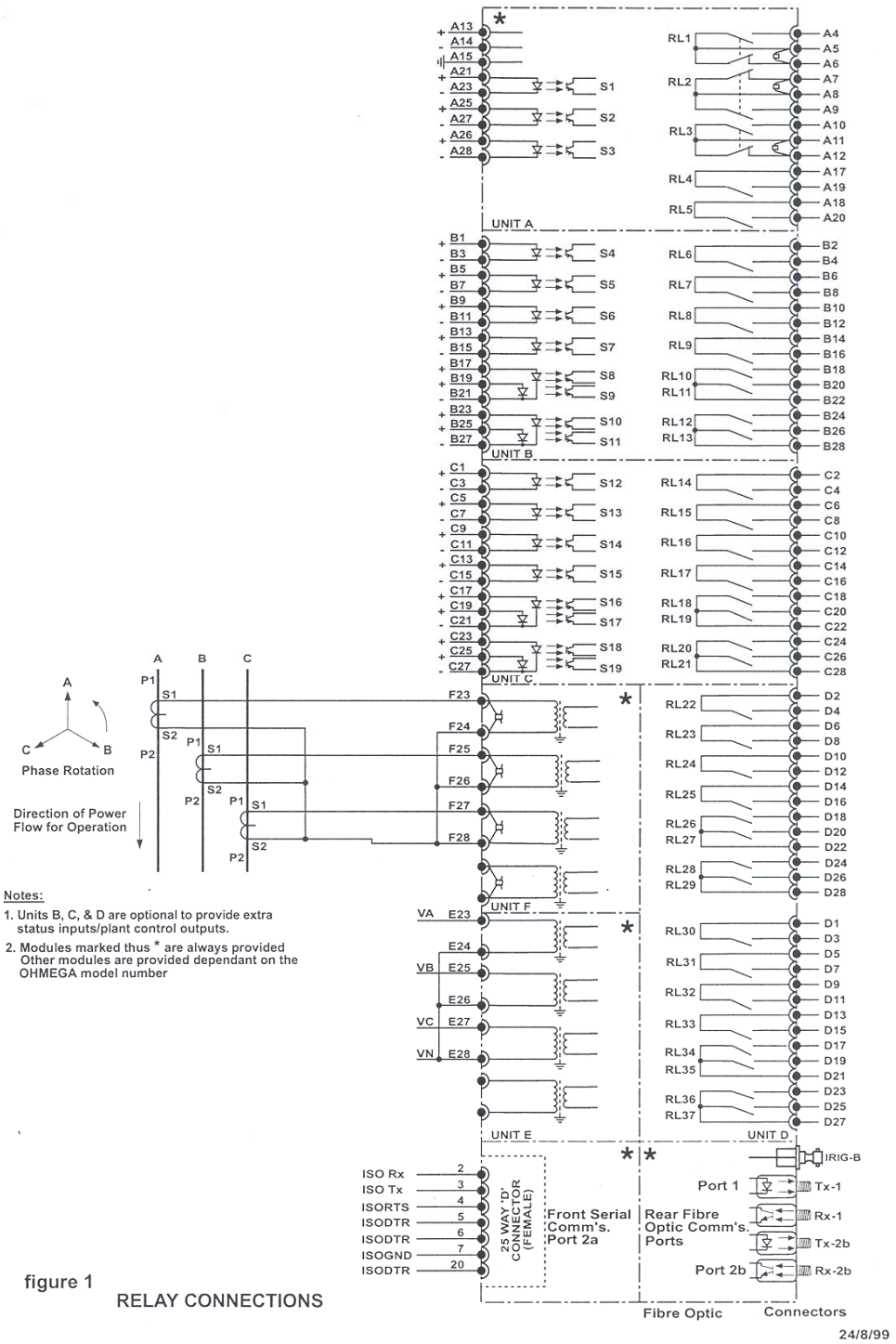


figure 1
RELAY CONNECTIONS

2 Overall dimensions and panel drilling for Epsilon E16

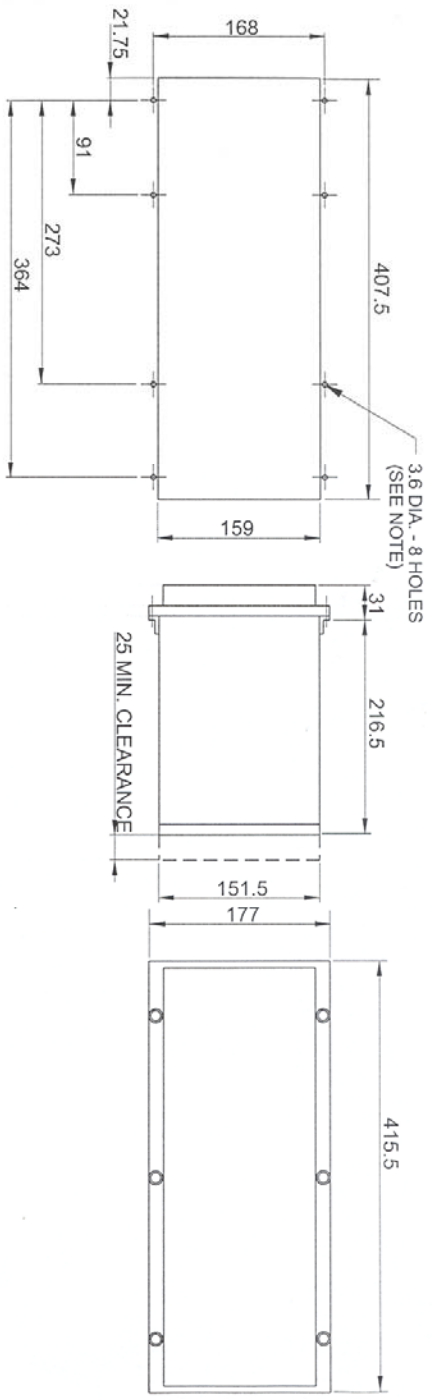


figure 2
OVERALL DIMENSIONS AND PANEL DRILLING FOR EPSILON E16 CASE

NOTE:
THE 3.6 DIA. HOLES ARE FOR M4 THREAD FORMING (TRILOBULAR) SCREWS. THESE ARE SUPPLIED AS STANDARD AND ARE SUITABLE FOR USE IN FERROUS/ALUMINIUM PANELS 1.6mm THICK AND ABOVE. FOR OTHER PANELS, HOLES TO BE M4 CLEARANCE (TYPICALLY 4.5 DIA.) AND RELAYS MOUNTED M4 MACHINE SCREWS, NUTS AND LOCKWASHERS (SUPPLIED IN PANEL FIXING KIT).

24/8/99

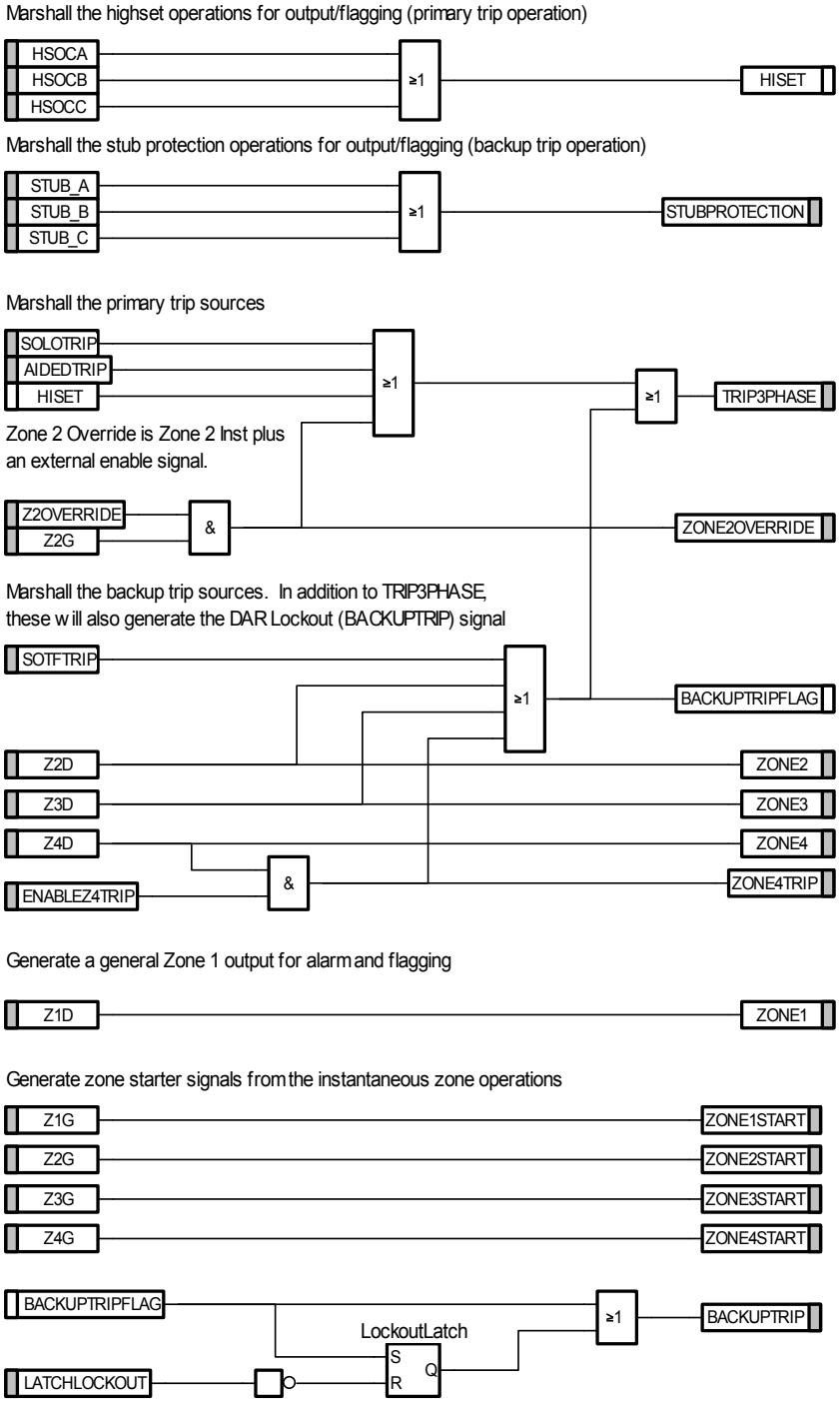
3 Reylogic Diagrams.

The following diagrams show the logic used in the relay. This is split up into three sections – firstly the logic used for the distance protection function, then the auxiliary function logic, then finally the scheme logic.

4 Distance Protection

4.1 Trip Outputs

Title Ohmega 402 Tripping Logic
Art No 2615S81133 Revision 5
Author Ken Nickerson
Revision History now in page properties.



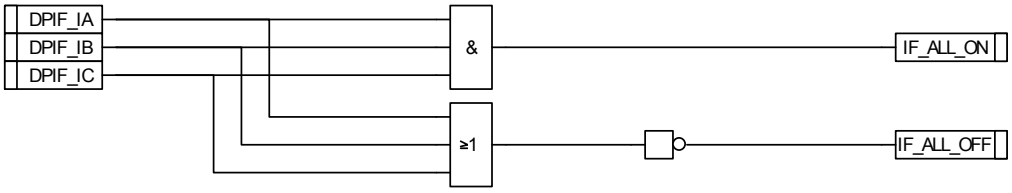
4.2 Voltage Memory

Title Voltage Memory Support
Art No 2615S81251
Author Ken Nickerson
See diagram properties for revision history

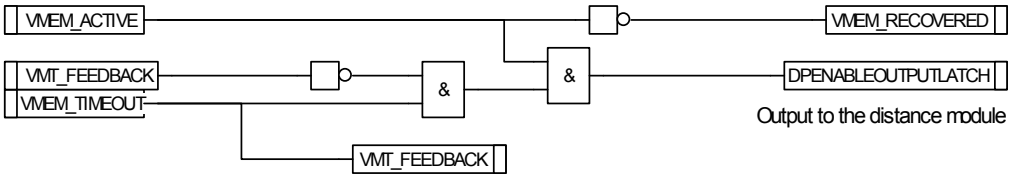
This diagram generates some control signals to latch/reset the zone1 and zone4 outputs when memory timeout occurs.

When a heavy three phase fault occurs, the fault voltage will collapse and the voltage memory will start timing out. After approx 100ms, the memory output will clamp off and the memory timeout signal will go active. This applies an inhibit to zone 1 and (where fitted) zone 4. The latch operation is required to prevent dropoff of the trip relays too early because of removal of of the comparator outputs. Reset occurs when memory recovers (voltage back) or the fault current is removed in all phases.

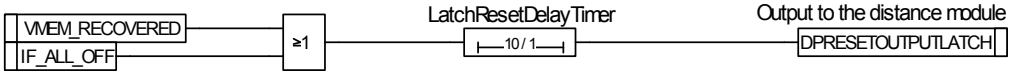
Firstly, we generate a reset control from the distance fault current detectors



Next, we generate the latch control signals for use by the distance module output latches - first the latch enable

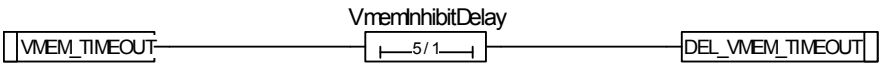


Now the latch reset signal

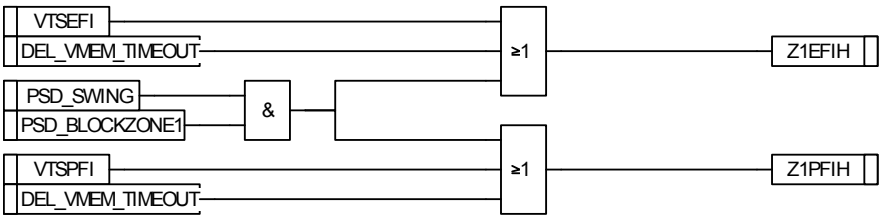


4.3 Trip Inhibit Logic

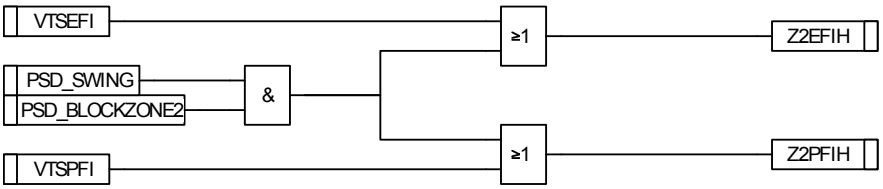
Title Ohmega 406 Inhibit Logic
Art No 2615S81237
Author Ken Nickerson



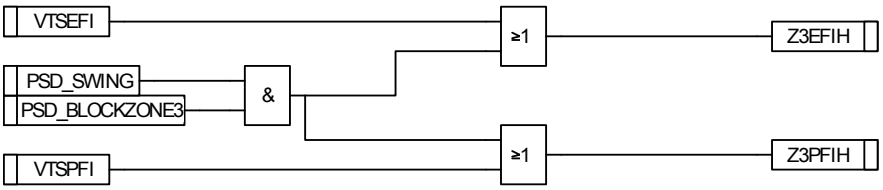
Allow Zone 1 to be inhibited by Power Swing, VTS, or Voltage Memory timing out.



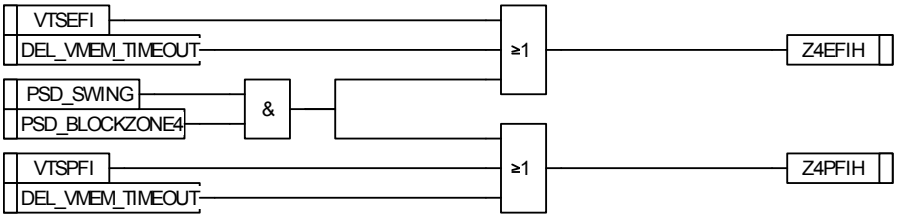
Allow Zone 2 to be inhibited by the same; Power Swing, VTS, or Vmem timed out.



Zone 3 has no memory voltage, so only inhibit from Power Swing and VTS



Zone 4 does have memory voltage, so inhibit from all, ie Power Swing, VTS, or Vmem timed out.



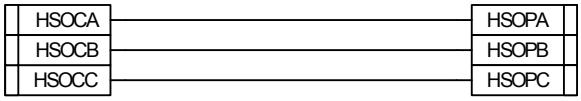
5 Auxilary Functions

5.1 High Set Overcurrent

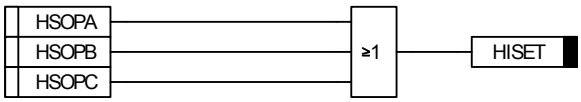
Title Hiset logic for Ohmega 400 series
Art No 2615S881235
Author Ken Nickerson

See Page Properties for revision history

Copy the protection output booleans to local bools for speed/safety



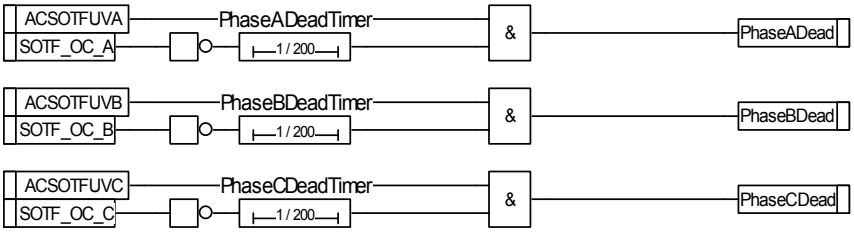
Generate an alarm output for the hiset. This is also used later as a 3 pole trip



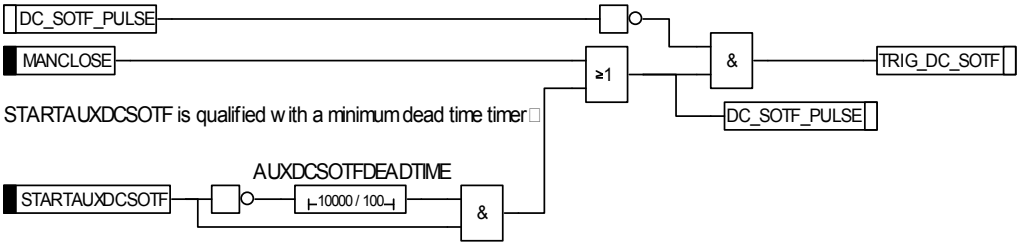
5.2 Switch-onto-Fault

Title Switch On To Fault
Art No 2615S81062
Author A Smith

First test each pole to see if it's 'dead'

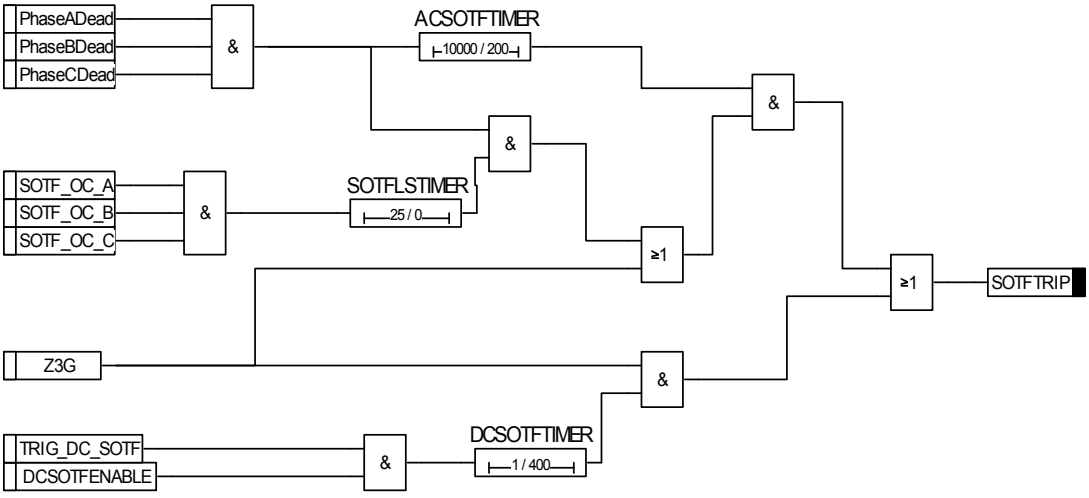


Generate a pulse from the manual close input.



STARTAUXDCSOTF is qualified with a minimum dead time timer

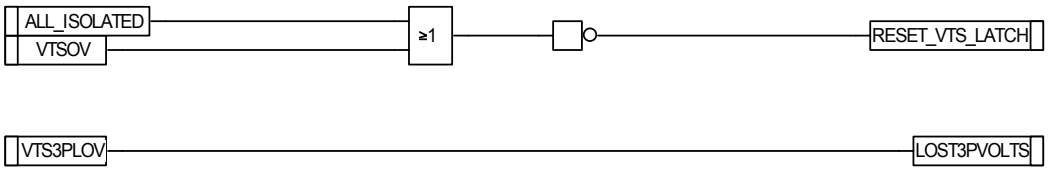
Now use this to evaluate the SOTF logic



5.3 Voltage Transformer Supervision

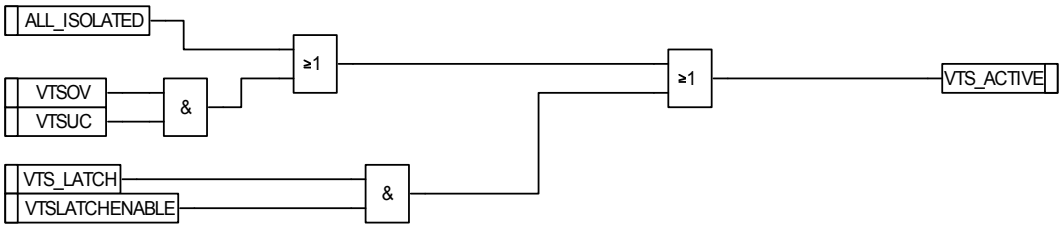
Title Voltage Transformer Supervision, version 2
Art No 2615S81153 R5
Author Ken Nickerson

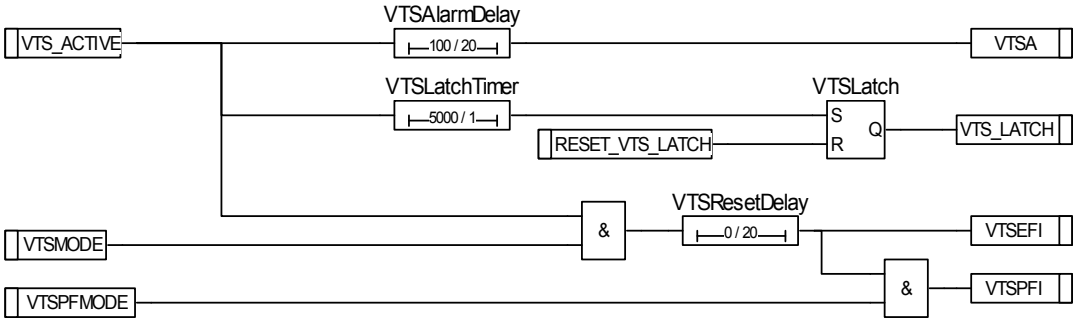
Generate the latch reset from the voltage recovery



Perform 3 pole loss of voltage check - gives alarm out only.

Now the actual VTS logic



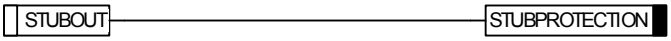


5.4 Stub Protection

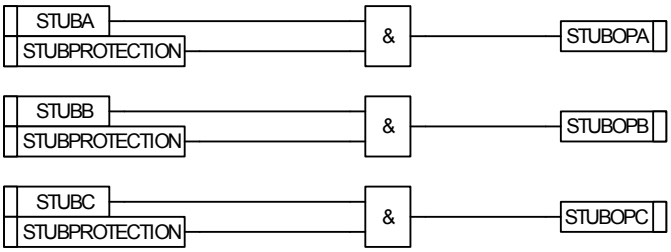
Title Stub protection logic for Ohmega 400 series
Art No 2615S81246
Author Ken Nickerson

See Page Properties for revision history

Generate an alarm/flag output for stub operation



Qualify the stub outputs for flagging.



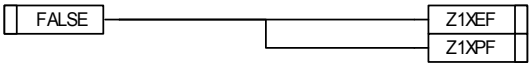
6 Protection Schemes

6.1 PUR

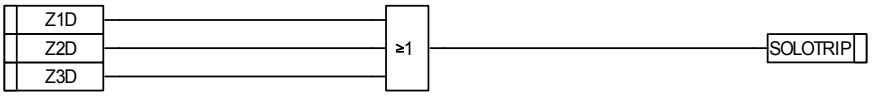
Title Permissive Underreach Scheme

Author Ken Nickerson

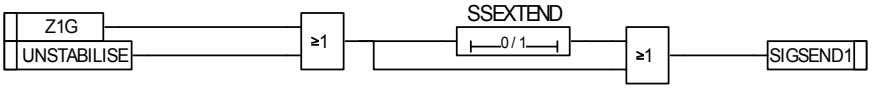
Clear the reach extension controls as that scheme is not in use.



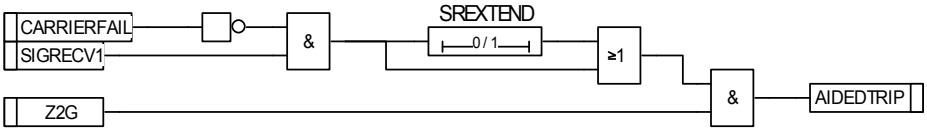
Plain tripping, generated by any delayed zone operation



Next, generate signal send from Zone 1 instantaneous, or the unstabilising input, which is either a manual operation, or comes from an external protection relay, giving us an intertrip



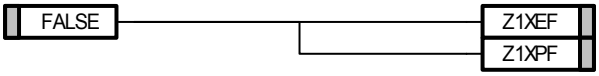
Finally, we generate our aided trip signal from signal receive 1, qualified by the lack of a carrier fail signal, stretch the resultant output and use it to qualify the instantaneous zone 2 output



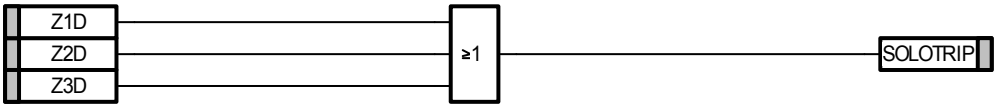
6.2 POR 1

Title Permissive Overreach Scheme using Zone 1
Art No 2615S81150
Author Ken Nickerson

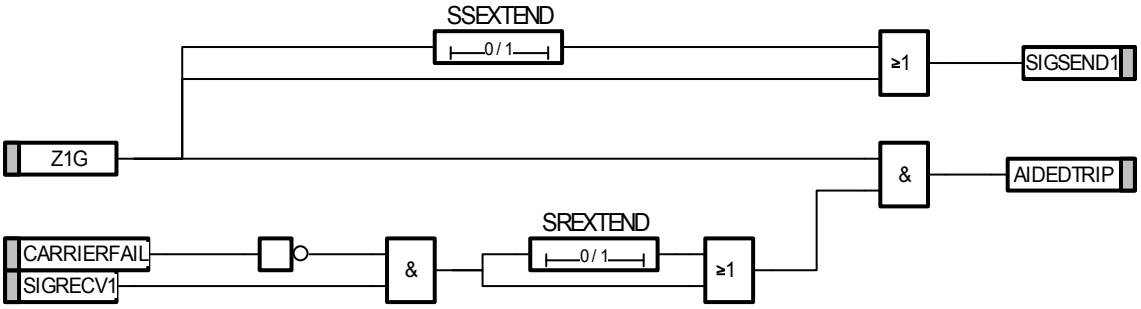
Clear the reach extension controls as that scheme is not in use.



Generate the general trip output from the delayed distance protection elements



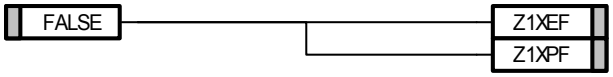
Now we generate the signal send from instantaneous zone 1, and the aided trip from zone 1 and stretched signal receive. We also incorporate the carrier fail input for security.



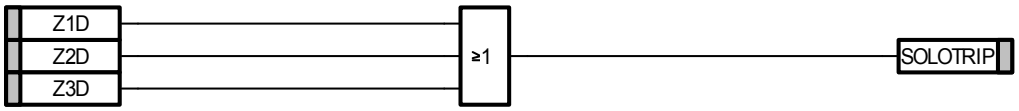
6.3 POR 2

Title Permissive Overreach Scheme using Zone 2
Art No 2615S81151
Author Ken Nickerson

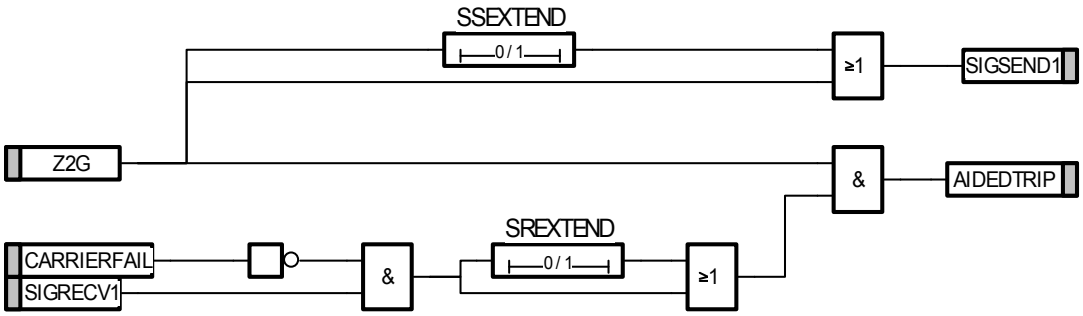
Clear the reach extension controls as that scheme is not in use.



Generate the general trip output from the delayed distance protection elements



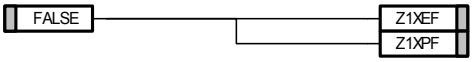
Now we generate the signal send from instantaneous zone 2, and the aided trip from zone 1 and stretched signal receive. We also incorporate the carrier fail input for security.



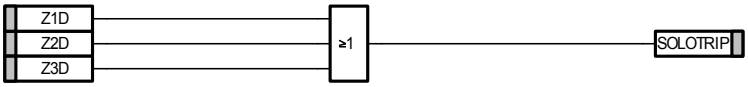
6.4 BOR

Title Blocking Overreach Type 2 Scheme using reverse Zone 4 for blocking and aided Zone 2 tripping
Art No 2615S81121
Author Ken Nickerson

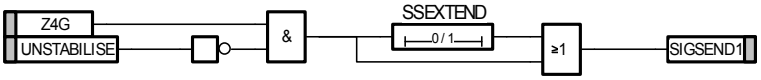
Clear the reach extension controls as that scheme is not in use.



Firstly, the general trip logic for normal zone operations



Next, we generate a blocking signal if Zone 4 operates. Zone 4 is reverse looking, so blocks out-of-zone (reverse) faults
Also, we add the external unstabilise control (Manual/external trip) into the equation to allow it to work with the scheme.



Now we generate the aided trip signal, which is delayed to allow time for blocking, and is blocked if signal receive is active.
Also, we need an inhibit signal to prevent blocking under certain circumstances, and to incorporate the carrier fail signal.

Also, generate an output tag so that the signal receive input can generate a flag